UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,816	02/25/2002	Andrew Cofler	00GR35154360	1555

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ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER
TSAI, HENRY

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	**Applicant(s)**
Office Action Summary	10/082,816	COFLER ET AL.
	Examiner	**Art Unit**	
	Henry W.H. Tsai	2181	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>02 February 2006</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>25-50</u> is/are pending in the application.

     4a) Of the above claim(s) __ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>25,30,36,38 and 50</u> is/are rejected.

7)☒ Claim(s) <u>26-29, 31-35, 37 and 39-49</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☒ All b)☐ Some * c)☐ None of:

        1.☒ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
     Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs

of 35 U.S.C. 102 that form the basis for the rejections under

this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or
> a foreign country or in public use or on sale in this country, more than one
> year prior to the date of application for patent in the United States.

2.   Claims 25, 36, 38, and 50 are rejected under 35

U.S.C. 102(b) as being anticipated by Underwood et al. (U.S.

Patent No. 5,928,357) (hereafter referred to as Underwood et

al.'357).

Referring to claim 25, Underwood et al.'357 discloses, as

claimed, a method of handling branching instructions using a

processor (see Fig. 1) comprising a program memory (250, see

Fig. 2) storing program instructions, and a processor core (10,

see Fig. 1) comprising a plurality of processing units

(certainly existing in the Underwood et al.'357's system, such

as integer unit, floating point unit, and addressing unit) and a

central unit (220, see Fig. 2) connected thereto, the central

unit issuing instructions to the processing units based upon the

program instructions, the method comprising: clocking the

processor core with a clock signal (<u>clock signal inputted to</u>

<u>program counter 260, see Fig. 2</u>); receiving a branching

instruction (<u>Instruction 3000B is fetched based on the branch</u>

<u>address, see Col. 3, lines 30-42, and Fig. 3</u>) in the course of a

current cycle (<u>clock cycle 370, see Fig. 3</u>); and processing the

received branching instruction in the current cycle (<u>see Fig. 3,</u>

<u>the branch instruction 3000B is fetched (see timing diagram</u>

<u>FDNXTI in Fig. 3) and executed (or processed) (see timing</u>

<u>diagram FDIR in Fig. 3) during phases 1 and 2 of the clock cycle</u>

<u>370</u>).

Referring to claim 36, Underwood et al.'357 discloses, as

claimed, a method of handling branching instructions using a

processor (<u>see Fig. 1</u>) comprising a program memory (<u>250, see</u>

<u>Fig. 2</u>) storing program instructions, and a processor core (<u>10,</u>

<u>see Fig. 1</u>) comprising a plurality of processing units

(<u>certainly existing in the Underwood et al.'357's system, such</u>

<u>as integer unit, floating point unit, and addressing unit</u>), and

a central unit (<u>220, see Fig. 2</u>) connected thereto, the central

unit issuing instructions to the processing units based upon the

program instructions, the method comprising: receiving at the

central core a branching instruction (<u>Instruction 3000B is</u>

fetched based on the branch address, see Col. 3, lines 30-42,
and Fig. 3) during a current clock cycle (clock cycle 370, see
Fig. 3) and processing the received branching instruction during
the current clock cycle (see Fig. 3, the branch instruction
3000B is fetched (see timing diagram FDNXTI in Fig. 3) and
executed (or processed) (see timing diagram FDIR in Fig. 3)
during phases 1 and 2 of the clock cycle 370).

Referring to claim 38, Underwood et al.'357 discloses, as
claimed, a processor (see Fig. 1) comprising: a program memory
(250, see Fig. 2) for storing program instruction; and a
processor core (10, see Fig. 1) being clocked by a clock signal
(see clock signal inputted to program counter 260, see Fig. 2)
and comprising a plurality of processing units (certainly
existing in the Underwood et al.'357's system, such as integer
unit, floating point unit, and addressing unit) and a central
unit (comprising such as ALU 220, see Fig. 2) connected thereto,
said central unit for issuing instructions to said processing
units based upon corresponding program instructions; said
central unit comprising a branching module (instruction register
240, see Fig. 2) for receiving a branching instruction
(Instruction 3000B is fetched based on the branch address, see
Col. 3, lines 30-42, and Fig. 3) during a current clock cycle
(clock cycle 370, see Fig. 3), and processing this branching

instruction during the current clock cycle (see Fig. 3, the

branch instruction 3000B is fetched (see timing diagram FDNXTI

in Fig. 3) and executed (or processed) (see timing diagram FDIR

in Fig. 3) during phases 1 and 2 of the clock cycle 370).

As to claim 50, Underwood et al.'357 also discloses: having

a decoupled architecture (since the instruction cycle of the

Underwood et al.'357's system comprises different pipelined

stages, see col. 2, lines 31-34, involving Instruction fetch or

prefetch and Operand fetch and using different units in the

different pipelined stages).

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which

forms the basis for all obviousness rejections set forth in this

Office action:

(a) A patent may not be obtained though the invention is not identically
disclosed or described as set forth in section 102 of this title, if the
differences between the subject matter sought to be patented and the prior
art are such that the subject matter as a whole would have been obvious at
the time the invention was made to a person having ordinary skill in the art
to which said subject matter pertains. Patentability shall not be negatived
by the manner in which the invention was made.

4.   Claim 30 is rejected under 35 U.S.C. 103(a) as being

unpatentable over Underwood et al.'357 in view of European

Patent Application No. EP 1 050 805 (hereafter referred to as

EP'805) or Applicant Admitted Prior Art mentioned in

Specification page 4, last paragraph to page 5, lines 1-18

(hereafter referred to as AAPA).

Underwood et al.'357 discloses the claimed invention except

for a second processing unit including a guard-indication

register, wherein in the presence of a guarded branching

instruction, a check on the validity of the guard indication

assigned to the branching instruction and contained in the

guard-indication register is carried out at the start of the

current cycle; and wherein the guarded branching instruction is

actually received by the central unit and processed, if the

value of the corresponding guard indication is declared valid,

and, in the opposite case, this guarded branching instruction is

kept on hold for processing until the value of the corresponding

guard indication is declared valid (in claim 30).

EP'805 discloses a system comprising a second processing

unit (19, see Fig. 1) contains a guard-indication register (100,

see Fig. 1), wherein in the presence of a guarded branching

instruction, a check on the validity of the value of the guard

indication assigned to said branching instruction (see Col. 5,

lines 54-55, regarding the guard selecting from G0-G15 selected

for each instruction (certainly including branch instruction))

and contained in the guard-indication register (100, see Fig. 1)

is carried out at the start of said current cycle, and in that

said guarded branching instruction is actually received by the

central unit (12, see Fig. 1) and processed, if the value of the

corresponding guard indication (see Col. 2, lines 44-49 or Col.

5, lines 54-55, regarding the guard selecting from G0-G15

selected for each instruction (certainly including branch

instruction)) is declared valid (see Col. 5, lines 56-58,

regarding the value true or false attributed to guards from G0-

G15 is however dependent upon the guard values held at any

particular time in a guard register file), and, in the opposite

case, this guarded branching instruction is kept on hold for

processing until the value of the corresponding guard indication

is declared valid. Besides, as Applicant Admitted Prior Art

mentioned in Specification page 4, last paragraph to page 5,

lines 1-18, the use of guarded instruction in a processor is

already known in to a person skilled in the art.

It would have been obvious to one having ordinary skill in

the art at the time the invention was made to modify Underwood

et al.'357's system to comprise a second processing unit

including a guard-indication register, wherein in the presence

of a guarded branching instruction, a check on the validity of

the guard indication assigned to the branching instruction and

contained in the guard-indication register is carried out at the

start of the current cycle; and wherein the guarded branching

instruction is actually received by the central unit and

processed, if the value of the corresponding guard indication is

declared valid, and, in the opposite case, this guarded

branching instruction is kept on hold for processing until the

value of the corresponding guard indication is declared valid,

as taught by EP'805 (or AAPA), in order to facilitate

efficiently controlling the branch instructions by reduce the

latency due to data dependency and pipeline stall problems (such

as using predicates, see Col. 1, lines 27-28), for the Underwood

et al.'357's device.

Allowable Subject Matter

5.   Claims 26-29, 31-35, 37, and 39-49 are objected to as being

dependent upon a rejected base claim, but would be allowable if

rewritten in independent form including all of the limitations

of the base claim and any intervening claims.

Response to Arguments

6.   Applicant's arguments mailed 2/2/06 have been considered

but are moot in view of the new explanation new ground(s) of
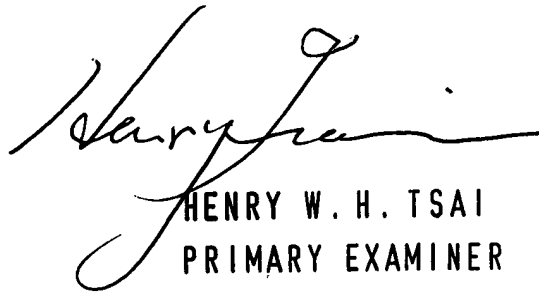
rejection.

Contact Information

7.   Any inquiry concerning this communication or earlier

communications from the examiner should be directed to Dr. Henry

Tsai whose telephone number is (571) 272-4176. The examiner can

normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful,

the examiner supervisor, Fritz M. Fleming, can be reached on

(571) 272-4145. Any inquiry of a general nature or relating to

the status of this application or proceeding should be directed

to **the TC central telephone number, 571-272-2100**.

8.   In order to reduce pendency and avoid potential delays,

Group 2100 is encouraging FAXing of responses to Office actions

directly into **the Group at fax number: 571-273-8300**. This

practice may be used for filing papers not requiring a fee. It

may also be used for filing papers which require a fee by

applicants who authorize charges to a PTO deposit account.

Please identify the examiner and art unit at the top of your

cover sheet. Papers submitted via FAX into Group 2100 will be

promptly forward to the examiner.

HENRY W. H. TSAI

PRIMARY EXAMINER

April 6, 2006